REMARKS

Claims 1-32 are pending in the present application, and stand rejected. Reconsideration of the rejections in view of the following is respectfully requested. This application continues to include claims 1-32.

The Examiner rejected claims 1-5, 10, 11, 16-19, 28-32 under the judicially created doctrine of obviousness-type double patenting in view of claims in the copending application 09/895,782. Claims 1, 10, 19 and 28 are independent. Claims 2-5 depend from claim 1; claims 11 and 16-18 depend from claim 10; and claims 29-32 depend from claim 28. As stated, "The Examiner notes that there [are] subtle variations in the claims but believes that the definitions are synonymous with the definitions of the original claims." The Examiner has indicated that a timely filed terminal disclaimer may be used to overcome this rejection.

Applicants respectfully submit, however, that the differences are more than subtle differences. In contrast to the claims of the copending application, for example, independent claim 1 of the present application requires the additional steps of "obtaining a communication link speed" and "calculating a sample count value of said counter using said communication link speed"; independent claim 10 of the present application recites, "determining a communication link speed" and "defining a sample count value of said counter utilizing said communication link speed"; independent claim 19 of the present application recites, "said speed input being adapted to receive a variable representative of a communication link speed and said clock signal input being adapted for receiving a clock signal, wherein said synchronous pulse generator processes said clock signal, said communication link speed and said difference signal to generate a synchronous pulse used for extracting data from said

AMENDMENTS TO THE DRAWINGS

The Examiner has required corrected drawings because of "numerous handwritten captions and labels." Enclosed herewith under a separate cover letter is a set of Formal Drawings to replace the informal drawings submitted at the time of filing the present application.

difference signal"; and independent claim 28 of the present application recites, "detecting a data speed" and "defining a sampling count value based on said data speed".

Also, as more fully set forth below, the differences identified above also contribute to the patentable distinctions of the claims over the cited references.

Thus, Applicants believe the claims of the present application differ in more than a subtle way from the claims of the copending application. Accordingly, it is respectfully requested that the obviousness-type double patenting rejection be withdrawn.

The Examiner has required corrected drawings because of "numerous handwritten captions and labels". Enclosed herewith under a separate cover letter is a set of Formal Drawings to replace the informal drawings submitted at the time of filing the present application.

Claims 28-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nimishakavi (U.S. Patent No. 5,594,763). Applicants respectfully request reconsideration in view of the following.

Claim 28 is directed to a method for synchronizing a receiver to data, comprising the steps of: detecting a data speed; initializing a counter to count clock cycles; detecting a current count value; defining a sampling count value based on said data speed; detecting a change in said data; incrementing said count value if no change in said data is detected; and, generating a pulse when said counter reaches said sampling count value. (Emphasis added).

Nimishakavi discloses a digital phase-locked loop for receiving an encoded stream of data and generating a receive clock signal. A DPLL clock signal is provided to a conventional data synchronizer 42 that receives at its other input the receive data signal Rx Data. The data synchronizer 42 produces from these signals a synchronized receive data signal (RxD Sync).

The synchronized received data signal (RxD Sync) is provided to an edge detector 46 that is enabled by a signal from an edge detector enable 44. Once enabled, when an edge is detected, the edge detector 46 provides a signal to a count load control circuit 50. Under the control of the count load control 50, the counter 40 will be loaded with the value contained in the count register 48 and begin counting down from that start count value. A negative count detector 54 is coupled to a down counter 40. A receive clock generator 52 is coupled to the down counter 40 and generates the receive clock signal (RxDPLL clock out) that is used to determine the sampling times of the received data signal, i.e., Rx Data. (See Nimishakavi, column 4, lines 22-50).

Thus, in Nimishakavi, two clock signals, i.e., the DPLL clock signal and the receive clock signal (RxDPLL clock out) are used, but it is the receive clock signal (RxDPLL clock out) that is used in sampling data. More particularly, the DPLL clock signal is used to generate the synchronized receive data signal (RxD Sync), and the DPLL clock signal is used to generate receive clock signal (RxDPLL clock out), but it is the "receive clock signal (RxDPLL clock out) that is used to determine the sampling times of the received data signal, i.e., Rx Data." (See Nimishakavi Fig. 4, column 4, lines 22-50; emphasis added).

Claim 28 recites detecting a data speed, and defining a sampling count value based on said data speed. While the Examiner asserts that Nimishakavi discloses "initializing a counter to count clock cycles", and "defining a sampling count value", nowhere does the Examiner assert that Nimishakavi discloses, teaches or suggested the above referenced aspects of claim 28, which Applicants contend are absent in Nimishakavi.

In contrast to claim 28, Nimishakavi discloses that. "An adjustable start count value, such as 31 or 15, may be loaded into a count register 48 by the CPU 12. The actual value

loaded into the count register is dependent upon the type of encoding of the received data. The value 31, for example, will be loaded if the data is NRZI encoded; while the value 15 will be loaded if the data is FM encoded. Under the control of the count load control 50, the counter 40 will be loaded with the value contained in the count register 48 and begin counting down from that start count value. In certain preferred embodiments of the present invention, the down counter is a 6-bit down counter." (Emphasis added). Thus, in Nimishakavi the count value is selected depending on the type of encoding, and does not disclose, teach or suggest defining a sampling count value based on said data speed, as recited in claim 28.

Accordingly, it is respectfully submitted that Nimishakavi does not render obvious claim 28.

Claims 29-32 are believed to be allowable due to their dependence from claim 28.

Accordingly, it is respectfully requested that the Examiner withdraw the rejection of claims 28-32 under 35 U.S.C. § 103(a) as being unpatentable over Nimishakavi.

Claims 1-19 and 22-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nimishakavi in view of IEEE P1394b Draft Standard for a High Performance Serial Bus (03/21/2001). Applicants respectfully request reconsideration in view of the following.

Claim 1 recites, in part, a method for effecting synchronous pulse generation for use in serial communications, wherein "if said current count value corresponds to said sample count value then performing a step of generating a synchronous pulse, and if said current count value does not correspond to said sample count value then performing a step of determining whether a signal level of said difference signal has changed, and if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal until said current count value of said counter corresponds to

said sample count value at which time said step of generating said synchronous pulse is repeated."

The Examiner relies on Nimishakavi Figs. 4 and 6, column 4, lines 33-43; column 4, line 65-column 5, line 6; column 5, lines 7-15; column 5, line 50-column 6, line 5; and column 6, lines 30-42, with regard to claim 1, while recognizing that Nimishakavi is silent on the generation of a difference signal (for which the Examiner relies on the IEEE P1394b Specification).

In Nimishakavi when an edge is detected, the counter counts down and when the count reaches a predefined value (i.e., 4), the edge detector 46 is enabled to detect an edge, thus going purely off of the counter. Thus, Nimishakavi looks for an edge to occur only within the count range of 4 to 0. (See Nimishakavi, column 5, lines 50-61).

In contrast to Nimishakavi, the invention as recited in claim 1 always looks for an edge, i.e., a change in the signal level of the difference signal, except from when an edge has occurred to until the count has reached the sample count value, and then starts looking for an edge. More specifically, as recited in claim 1, if the signal level of said difference signal has changed (i.e., an edge detected), then further changes in the signal level of the difference signal are ignored until the current count value of the counter corresponds to the sample count value, at which time the step of generating the synchronous pulse is repeated. Thus, the present invention as recited in claim 1 does not utilize a count range within which an edge is looked for, as required by Nimishakavi, and the distinction of the present invention from Nimishakavi is not overcome by the IEEE P1394b Specification.

Further, the cited references, taken alone or in combination, do not disclose, teach or suggest obtaining a communication link speed and calculating a sample count value of said counter using said communication link speed, as asserted by the Examiner.

The Examiner asserts the step of "obtaining a communication link speed" is disclosed in Nimishakavi at column 4, lines 33-43; however, the cited passage from Nimishakavi is totally silent on obtaining a communication link speed. Rather, Nimishakavi at column 4, lines 33-43, states, "An adjustable start count value, such as 31 or 15, may be loaded into a count register 48 by the CPU 12. The actual value loaded into the count register is dependent upon the type of encoding of the received data. The value 31, for example, will be loaded if the data is NRZI encoded; while the value 15 will be loaded if the data is FM encoded. Under the control of the count load control 50, the counter 40 will be loaded with the value contained in the count register 48 and begin counting down from that start count value. In certain preferred embodiments of the present invention, the down counter is a 6-bit down counter." Accordingly, nowhere in the cited passage does Nimishakavi disclose, teach or suggest "obtaining a communication link speed", as recited in claim 1.

Further, the Examiner asserts the step of "defining (where this is interpreted as a calculation) a sample count value of a counter" is disclosed in Nimishakavi at Figure 6,(f), but does not assert that Nimishakavi discloses "calculating a sample count value of said counter using said communication link speed", as recited in claim 1. In any event, Nimishakavi at Figure 6,(f) merely discloses a counter signal, which in no way characterizes "calculating a sample count value of said counter", let alone "calculating a sample count value of said counter using said communication link speed", as recited in claim 1. Accordingly, nowhere in the cited portion of Nimishakavi is there any disclosure, teaching or suggestion of "calculating

a sample count value of said counter using said communication link speed", as recited in claim 1.

The above-identified distinctions with respect to Nimishakavi are not overcome by the IEEE P1394b Specification.

Accordingly, for the above reasons, claim 1 is believed to be patentable in its present form.

Claims 2-9 depend, directly or indirectly, from claim 1. Accordingly, claims 2-9 are believed to be patentable in view of their dependence from claim 1, for the reasons set forth above with respect to claim 1. In addition, claims 2-9 further and patentably define the present invention over the cited references.

Independent claim 10 is believed to be patentable for substantially the same reasons set forth above with respect to claim 1.

Claims 11-18 depend, directly or indirectly, from claim 10. Accordingly, claims 11-18 are believed to be patentable in view of their dependence from claim 10. In addition, claims 11-18 further and patentably define the present invention over the cited references.

Claim 19, recites in part "a synchronous pulse generator having a first difference signal input, a clock signal input, a speed input and a synchronous pulse output, said difference signal input being coupled to said first output for receiving said difference signal, said speed input being adapted to receive a variable representative of a communication link speed and said clock signal input being adapted for receiving a clock signal, wherein said synchronous pulse generator processes *said clock signal, said communication link speed and said difference signal* to generate a synchronous pulse used for extracting data from said difference signal." (Emphasis added).

In rejecting claim 19, the Examiner relies on Nimishakavi at Figure 4, elements 40 and 48, as disclosing "said speed input being adapted to receive a variable representative of a communication link speed". Applicants find no support in Nimishakavi to draw such a conclusion. In particular, Nimishakavi discloses at column 4, lines 14-21, a down counter 40 that receives the digital phase-locked loop clock (DPLL clock), which is some multiple of the received data signal (Rx Data), from the clock divider network 38. Nimishakavi discloses at column 4, lines 33-43 that, "An adjustable start count value, such as 31 or 15, may be loaded into a count register 48 by the CPU 12. *The actual value loaded into the count register is dependent upon the type of encoding of the received data.* The value 31, for example, will be loaded if the data is NRZI encoded; while the value 15 will be loaded if the data is FM encoded. Under the control of the count load control 50, the counter 40 will be loaded with the value contained in the count register 48 and begin counting down from that start count value. In certain preferred embodiments of the present invention, the down counter is a 6-bit down counter." (Emphasis added). However, nowhere in Nimishakavi is there any indication of "said speed input being adapted to receive a variable representative of a communication link speed", as recited in claim 19.

In addition, the cited references do not disclose, teach or suggest a synchronous pulse generator that processes the clock signal, *the communication link speed* and the difference signal to generate a synchronous pulse used for extracting data using said clock signal, as recited in claim 19. In contrast, the IEEE P1394b Specification is silent on the issue, and Nimishakavi uses the receive clock signal (RxDPLL clock out) to sample data. More particularly, the DPLL clock signal is used to generate the synchronized receive data signal (RxD Sync), and the DPLL clock signal is used to generate receive clock signal (RxDPLL

clock out), but it is the "receive clock signal (RxDPLL clock out) that is used to determine the sampling times of the received data signal, i.e., Rx Data." (See Nimishakavi Fig. 4, column 4, lines 22-50; emphasis added). Thus, Nimishakavi uses the receive clock signal (RxDPLL clock out), and not RxD Sync, to determine the sampling times of the received data signal, i.e., Rx Data.

Further, the Examiner does not assert that Nimishakavi discloses a synchronous pulse generator that processes three signals, i.e., the clock signal, *the communication link speed* and the difference signal, to generate a synchronous pulse used for extracting data from the difference signal, as recited in claim 19. Rather, the Examiner asserts that the synchronous pulse generator processes a clock signal and a data signal to generate a synchronous pulse. Accordingly, the rejection of claim 19 is lacking in this regard as well.

The above-identified distinctions with respect to Nimishakavi are not overcome by the IEEE P1394b Specification.

In view of the above, Applicants believe claim 19 is patentable in its present form.

Claims 22-23 depend, directly or indirectly, from claim 19. Accordingly, claims 22-23 are believed to be patentable in view of their dependence from claim 19. In addition, claims 22-23 further and patentably define the present invention over the cited references.

For example, claim 22 recites, "The variable speed communications device of claim 19, wherein said synchronous pulse generator includes a speed register for storing a speed value that corresponds with a communication speed of a serial bus." In rejecting claim 22, the Examiner relies on Nimishakavi, Fig. 4, element 48. However, nothing in Nimishakavi supports the Examiner's "interpretation" of Nimishakavi element 48. Nimishakavi discloses at column 4, lines 33-43 that "An adjustable start count value, such as 31 or 15, may be loaded

into a count register 48 by the CPU 12. The actual value loaded into the count register is dependent upon the type of encoding of the received data. The value 31, for example, will be loaded if the data is NRZI encoded; while the value 15 will be loaded if the data is FM encoded. Under the control of the count load control 50, the counter 40 will be loaded with the value contained in the count register 48 and begin counting down from that start count value. In certain preferred embodiments of the present invention, the down counter is a 6-bit down counter." However, nowhere in Nimishakavi is there any indication of a synchronous pulse generator that includes a speed register for storing a speed value that corresponds with a communication speed of a serial bus, as recited in claim 22.

Accordingly, claim 22 is believed patentable in its own right.

Accordingly, it is respectfully requested that the Examiner withdraw the rejection of claims 1-19 and 22-23 under 35 U.S.C. § 103(a) as being unpatentable over Nimishakavi in view of the IEEE P1394b Draft Standard for a High Performance Serial Bus (03/27/2001).

Claims 20, 21, and 24-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nimishakavi in view of IEEE P1394b, and in further view of Ryan (U.S. Patent No. 6,169,501). Applicants respectfully request reconsideration in view of the following.

The Examiner acknowledges that Nimishakavi is silent with respect to a serial/parallel translator, 8B/10B decoder, and descrambler, but contends that Nimishakavi "does state that his device is to be used to sample data." The Examiner further asserts, however, that Ryan teaches the addition of a serial/parallel translator. Applicants respectfully disagree.

Ryan is directed to an adjustable serial-to-parallel or parallel-to-serial converter. "The sample clock synchronization logic for receiving an asynchronous data signal as described in

FIGS. 1-5 and the data converters as described in FIGS. 6-8 may be used in conjunction in a device for receiving and/or transmitting asynchronous data. For example, the sample clock synchronization logic of FIG. 5 may be used to determine when to sample serial data signal 10 to provide that data as the serial data input 110 to the data converter of FIG. 7 or 8. Sample clock 16 may be used to determine when to clock the shift registers of the data converter so that a valid data bit of the serial data signal 10 is shifted in as the serial data input 110 into the first shift register of the data converter. Also, the converter of FIG. 6 or 8 may be used to convert parallel data to serial data to be transmitted in a serial data communication system or application." (See Ryan, column 14, lines 16-30; emphasis added).

Claim 20 recites, in part "a serial/parallel translator having a second difference signal input, a synchronous pulse input and an encoded data output, said second difference signal input being connected to said first difference signal input for receiving said difference signal and said synchronous pulse input being connected to said synchronous pulse output for receiving said synchronous pulse, and said serial/parallel translator processing said difference signal and said synchronous pulse *to generate encoded data*, said *encoded data being output on said encoded data output*". (Emphasis Added).

With respect to claim 20, the Examiner asserts that Ryan teaches a serial/parallel translator having a second data signal, a synchronous pulse input and a parallel output. However, this is not what is recited in claim 20. Rather, claim 20 recites a serial/parallel translator having a second difference signal input, a synchronous pulse input and an encoded data output. Ryan does not disclose, teach or suggest using a second difference signal input, nor does Ryan disclose, teach or suggest generating an encoded output. As such, the

combination of Ryan with IEEE1394b, as asserted by the Examiner, would not yield Applicants' invention, as recited in claim 20.

The Examiner asserts that Ryan Fig. 7, 112 discloses a synchronous pulse input for receiving the synchronous pulse. In this regard, Ryan states at column 13, lines 25-30 that, "When the serial data has been shifted in to the desired parallel data word length, control logic 104 asserts out signal 112 which causes parallel data word out logic 90 to accept a bit of the parallel data word from the output of each of the flip-flops 96 in parallel." However, in each of claims 20 and 24, for example, the serial/parallel translator processes the synchronous pulse, along with at least one other signal, "to generate encoded data *for output* on said encoded output." In contrast, out signal 112 of Ryan merely transfers the generated parallel data from the flip-flops in parallel at a particular time, and does not disclose using out signal 112 to generate encoded data.

For reasons set forth above, claim 20 is believed patentable in its own right.

In addition, claims 20 and 21 are believed patentable due to their dependence from claim 19, since the introduction of the Ryan reference does not overcome the deficiencies of Nimishakavi and the IEEE P1394b Specification with respect to claim 19.

Independent claim 24 recites, among other things, "a serial/parallel translator having a second clock input, a second difference signal input, a synchronous pulse input and an encoded data output, said second clock input being coupled to said first clock input for receiving said clock signal, said second difference signal input being connected to said first difference signal input for receiving said difference signal and said synchronous pulse input being connected to said synchronous pulse output for receiving said synchronous pulse,

wherein said serial/parallel translator processes said clock signal, said difference signal and said synchronous pulse *to generate encoded data* for output on said encoded data output."

The Examiner asserts that Ryan teaches a serial interface engine processing a data signal and synchronous pulse to generate parallel data for output on a parallel output, relying of Ryan Figure 7, elements 110, 96, 90, out signal 112, and column 13, lines 22-39. This language, however, does not appear in claim 24, which recites that "said serial/parallel translator processes said clock signal, said difference signal and said synchronous pulse *to generate encoded data* for output on said encoded data output." In contrast, out signal 112 of Ryan merely transfers the generated parallel data from the flip-flops in parallel at a particular time, and does not disclose using out signal 112, or elements 110, 96, 90, to generate encoded data.

In addition, the Examiner asserts that Nimishakavi discloses with respect to Fig. 4 a clock signal DPLL Clock. Claim 24 recites receiving "said clock signal" at the clock input of the serial/parallel translator. In contrast, for example, Nimishakavi discloses a RxDPLL ClkOut, derived from the DPLL Clk (the clock), which may be used as an output to another device (see Nimishakavi Fig. 4), rather than the DPLL Clk (said clock).

Accordingly, claim 24 is believed patentable in its present form.

Claims 25-27 depend, directly or indirectly, from claim 24. Accordingly, claims 25-27 are believed to be patentable in view of their dependence from claim 24. In addition, claims 25-27 further and patentably define the present invention over the cited references.

Accordingly, in view of the above, it is respectfully requested that the Examiner withdraw the rejection of claims 20, 21, and 24-27 under 35 U.S.C. § 103(a) as being unpatentable over Nimishakavi in view of IEEE P1394b, and in further view of Ryan.

For the foregoing reasons, Applicants submit that the present application is in condition for allowance in its present form, and it is respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefor and authorize that any charges be made to Deposit Account No. 20-0095, TAYLOR & AUST, P.C.

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (317) 894-0801.

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